REMARKS

Reconsideration of the application as amended is respectfully requested.

Claims 26-30 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 6,188,253 of Gage et al. ("Gage").

Claims 26-30 have been canceled. New claims 31-34 have been added. The new claims are supported by the specification at pages 75-79, Figure 24, and the originally filed claims. It is respectfully submitted that the new claims do not add new matter.

Applicants reserve all rights with respect to the applicability of the doctrine of equivalents.

The specification has been amended at page 77, line 12 to correct an obvious error. Support for the correction is found in the specification at page 77, lines 9-16. It is respectfully submitted that the correction does not add new matter.

The Examiner has rejected claim 26 under 35 U.S.C. § 102(b) as being unpatentable over Gage. The Examiner has stated the following:

> With respect to claim 26, Gage et al. (hereinafter Gage) teaches a clocking apparatus for an electronic tester, comprising:
>
> a first high speed clock generator coupled to a digital test circuit (see col. 4, lines 32-44 and FIG. 5A), wherein the first high speed clock generator generates a first clock having a first frequency that is a first multiple of an input frequency (see col. 4 line 60 to col. 5 line 3 and col. 5, lines 48-60).
>
> a second high speed clock generator coupled to an analog test circuit (see col. 4, lines 25-31 and FIG. 5A), wherein the second high speed clock generator generates a second clock having a second frequency that is a second multiple of the input frequency (see col. 4, lines 25-31).

a reference frequency clock source (see col. 4 line 67 to col. 5 line 12);

a variable clock generator coupled to the reference frequency clock source and coupled to the first and second high speed clock generators, wherein the variable clock generator has a continuously adjustable clock frequency that determines the input frequency for the first and second high speed clock generators (see col. 6, lines 1-17).

(6/29/05 Office Action pp. 1-2).

Claim 26 has been canceled.

Applicants submit that the present application is entitled to a priority date of October 30, 1998 based on grandparent application number 09/183,038. Gage issued February 13, 2001, so Gage is not prior art under 35 U.S.C. § 102(b) to the present application. Gage has a filing date of October 7, 1998, so the Examiner is apparently relying on 35 U.S.C. § 102(e), not 35 U.S.C. § 102(b), for the rejection.

Applicants reserve all rights to swear behind Gage. Nevertheless, applicants respectfully submit that new claim 31 is not anticipated by Gage under 35 U.S.C. § 102(e).

New claim 31 reads as follows:

a clocking apparatus for an electronic tester, comprising:

a fixed frequency clock generator that generates a first clock;

a variable frequency clock generator that receives as an input the first clock from the fixed frequency clock generator and that generates a second clock;

a first high speed clock generator coupled to a digital pattern generator for digital testing of a device under test, wherein the first high speed clock generator receives as an input the second clock from the variable frequency clock generator and generates a third clock having a frequency that is a first multiple

> of a frequency of the second clock, wherein the third clock is supplied to the digital pattern generator;
>
> a second high speed clock generator coupled to a sequenced measure system for analog testing of the device under test, wherein the second high speed clock generator receives as an input the first clock from the fixed frequency clock generator and generates a fourth clock having a frequency that is a second multiple of a frequency of the first clock, wherein the fourth clock is supplied to the sequenced measure system.

(Claim 31).

Gage discloses an analog clock module 50 that includes a direct digital synthesizer (DDS) 52 to generate an analog waveform from a digital clock source 48 (Gage col. 4, lines 25-28). The analog output from the DDS 52 is then fed to a signal conditioner 63 comprised of several signal conditioning components (Gage col. 4, lines 45-48). The analog output first passes through a bandpass filter (Gage col. 4, lines 48-50). After that, the filtered analog output feeds a clipping amplifier 66 (Gage col. 4, lines 55-56). A phase lock loop circuit multiplies the frequency of the analog output of the clipping amplifier 66 to level within the range of about 64 MHz to 100 MHz (Gage col. 4, lines 60-64). A divider 70 then reduces the PLL multiplied frequency to a desired level and outputs analog clock output 32. (Gage col. 4, line 67 to col. 5, line 3). A prediction processor 72 produces a digital event signal indicator ACLK as an output. (Gage col. 5, lines 16-19; col. 6, line 60, and Figure 3). In short, Gage discloses circuitry for producing an analog clock signal from a digital clock source.

In contrast to new claim 31, Gage does not disclose the following limitations of new claim 31:

> a first high speed clock generator coupled to a digital pattern generator for digital testing of a device

under test, wherein the first high speed clock generator receives as an input the second clock from the variable frequency clock generator and generates a third clock having a frequency that is a first multiple of a frequency of the second clock, wherein the third clock is supplied to the digital pattern generator;

a second high speed clock generator coupled to a sequenced measure system for analog testing of the device under test, wherein the second high speed clock generator receives as an input the first clock from the fixed frequency clock generator and generates a fourth clock having a frequency that is a second multiple of a frequency of the first clock, wherein the fourth clock is supplied to the sequenced measure system.

(New claim 31).

Gage teaches away from new claim 31 because Gage does not disclose two high speed clock generators, wherein one supplies a clock to a digital pattern generator, the other supplies a clock to a sequenced measure system.

Applicants therefore respectfully submit that new claim 31 is not unpatentable under 35 U.S.C. § 102(e) in view of Gage.

The Examiner has rejected claims 27-30 under 35 U.S.C. § 102(b) as being unpatentable over Gage.

Claims 27-30 have been canceled.

Given that claims 32-34 are dependent claims with respect to claim 31 and add further limitations, applicants respectfully submit that claims 32-34 are not unpatentable under 35 U.S.C. § 102(e) in view of Gage.

Applicants submit that submit that U.S. Patent No. 6,232,759 of Wohlfarth ("Wohlfarth") is not prior art to the present application given that the priority date of the present application is October 30, 1998. Wohlfarth issued May 15, 2001 based on an

application filed October 21, 1999, and those dates are all later than the priority date of the present application.

Applicants therefore respectfully submit that the rejections set forth in the Office Action have been overcome.

If there are any charges not covered by any check submitted, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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